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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/092,714	03/06/2002	Eric S. Fetzer	10016694-1	2508

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EXAMINER	
COLEMAN, ERIC	
ART UNIT	**PAPER NUMBER**
2183	

DATE MAILED: 08/27/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/092,714	FETZER ET AL.	
	Examiner	Art Unit	
	Eric Coleman	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-7 and 9-11* is/are rejected.

7)☒ Claim(s) *3 and 8* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1,2,4-7,9-11 are rejected under 35 U.S.C. 102(b) as being anticipated by Kimura (patent No. 6,105,127).

3. Kimura taught the invention as claimed including a data processing ("DP") system comprising: Multiple dispatch processor (e.g., see figs. 1,2,8,9,11,13,15 and col. 1, line 31-col. 6, line 30) comprising:

a) Plurality of fetch units (501 within fetch control unit 140) each instruction fetch unit capable of fetching a stream of instructions (e.g., see fig.1, 2, and col. 1, lines 21-67);

b) Plurality of decode units (502,111) and dispatch units (150) coupled to the corresponding fetch unit of the plurality of fetch units to receive instructions therefrom (e.g., see figs. 1,2,8) The corresponding decode units and dispatch units are drawn as connected in parallel for separate corresponding streams (e.g., see figs. 1,2,8) therefore although in figure 2 the dispatch or issue units are drawn together as one rectangular box, they would also be equivalently drawn as three separate dispatch boxes that operate with the corresponding decode unit. This parallel operation of the decode units and dispatch units are equivalent to

parallel decode and dispatch units (i.e., parallel units each with decode and dispatch units);

c) At least one register file (131,132,133,170,506) coupled for storing operands (e.g., see figs. 2,15);

d) Plurality of execution units (20,21,22,23) coupled to the register file and to the instruction decode and dispatch units for performing operations on operands as directed by the plurality of instruction decode units and dispatch units and a resource (e.g., see fig. 2);

e) Resource allocation unit (60) coupled to allocate execution units among the instruction decode and dispatch units (e.g., see figs.2,13 and col. 14, line 53-col. 16, line 44, and col. 17, lines 46-57).

4. As per claim 2, Kimura taught the instruction and dispatch units are capable of dispatching multiple instructions in a clock cycle (as a dispatch and decode unit is selected the output of the selected decode unit is de-multiplexed to send instructions to plurality of execution units in the same cycle (e.g., see figs. 8, 9).

5. As per claim 4, Kimura taught system the execution units comprised plural floating point units (e.g., see col. 7, line 58-col. 8, line15).

6. As per claims 5,6 Kimura taught the resource allocation unit dynamically allocating the execution units to instruction decode and dispatch units on a priority basis using individual settings for each decode and dispatch unit (e.g., see figs. 4, 8, 9, 10a, 10b, 10c, 11, 13, 15 and col. 8, line 17-col. 9, line 35).

7. As per claim 7, Kimura taught the resource allocation unit comprising resource available register for designating available resources (e.g., see col. 13, lines 32-44).

8. As per claim 9, Kimura taught apparatus for receiving resource requests from a plurality of instruction an decode and dispatch units (the configuration of the decode and dispatch units are discussed above in the discussion of claim 1) and for granting a plurality of resources to the decode and dispatch units (e.g., see figs. 8 , 9,,13,15 and col.2, line 60–col. 6, line 30).

9. As per claims 10,11 Kimura taught priority register (PRI, 61)(e.g., see fig.13 and col. 9,line 14-col. 11, line 51; and col. 14, line 54-col. 15, line 17), available register and marking the resources unavailable (e.g., see col. 13, lines 32-44).

Allowable Subject Matter

10. Claim 3,8 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Greenley (patent No. 5,761,469) disclosed a system for optimizing signed and unsigned load processing in a pipelined processor (e.g., see abstract).

Tremblay (patent No. 6,349,381) disclosed a pipelined instruction dispatch unit in a superscalar processor (e.g., see abstract).

Dubey (patent No. 5,724,565) disclosed a system for processing first and second sets of instructions by first and second types of processing systems (e.g. see abstract).

Soni (patent No. 6,742,111) disclosed a system with reservation stations to increase instruction level parallelism (e.g., see abstract).

Motomura (patent No. 5,944,811) disclosed a superscalar processor with parallel issue and execution device having forward map of operand an instruction dependencies (e.g., see abstract).

Any inquiry concerning this communication or earlier communications from the examiner should be `directed to Eric Coleman whose telephone number is (703) 305-9674 or (571) 272-4163. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703) 305-9712. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ERIC COLEMAN
PRIMARY EXAMINER

EC